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Seminario di fine I anno

XXX ciclo di Dottorato in Fisica e Astronomia

Innovative analog and mixed-signal solutions for precise measurement of electrical quantities in power transistors

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Outline

- Research objective
- Conversion system
- Design steps
    1) Mathematical model
    2) Transistor level implementation
- Results
- Future outlook

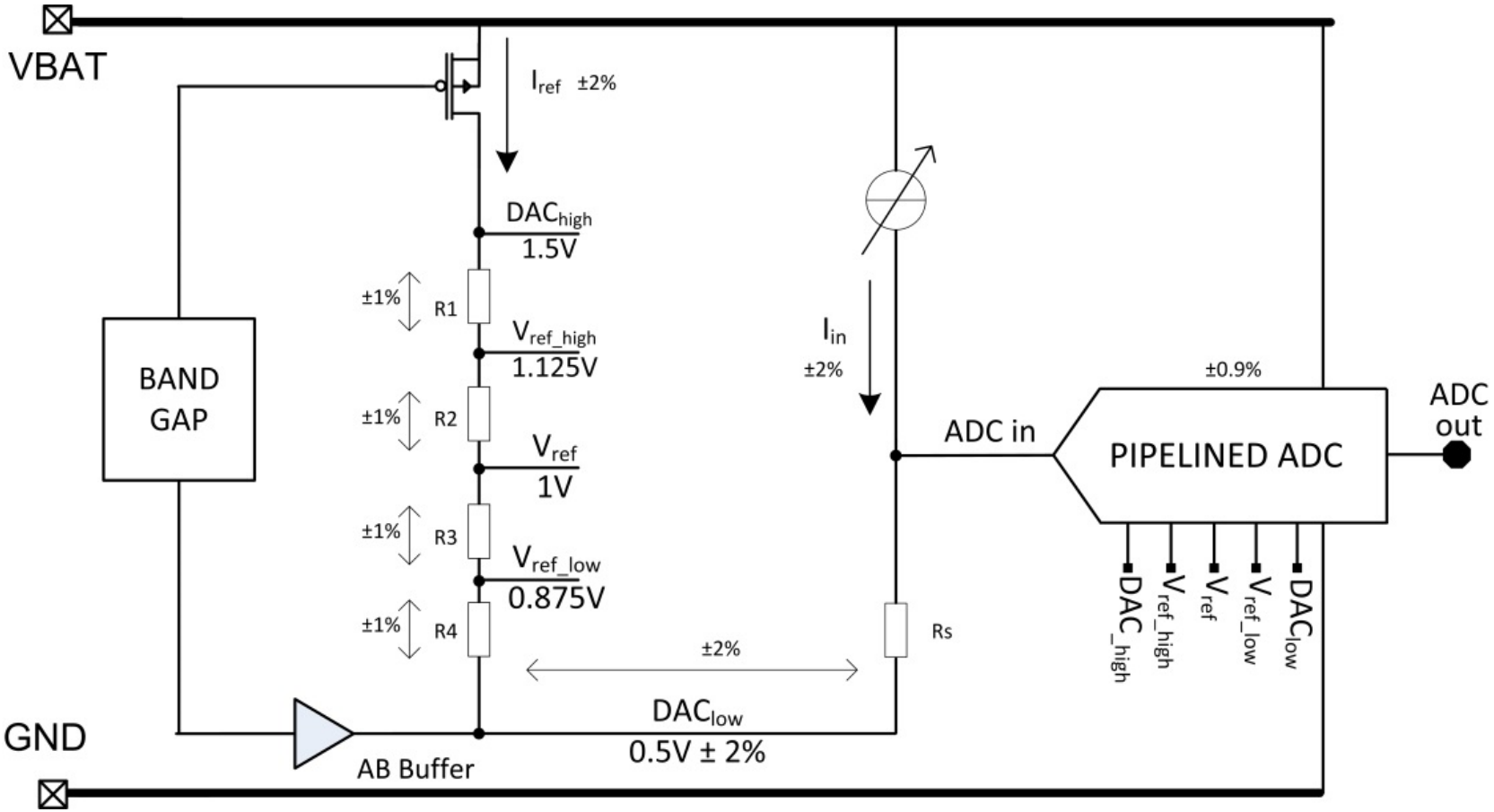
Research objective

System to be implemented

- Convert an input current I_{in} from analog to digital
- Integrate a low-voltage ADC alongside the power device
    1) Make use of a Smart-Power technology
- Requirements
    1) Distinguish I_{in} between 50µA and 100µA
    2) Accuracy for I_{in} = 5mA ≥ +/- 96%
    3) Continuous measuring range between 100µA and 10mA
    4) Current consumption <100µA
    5) Conversion time < 10µs

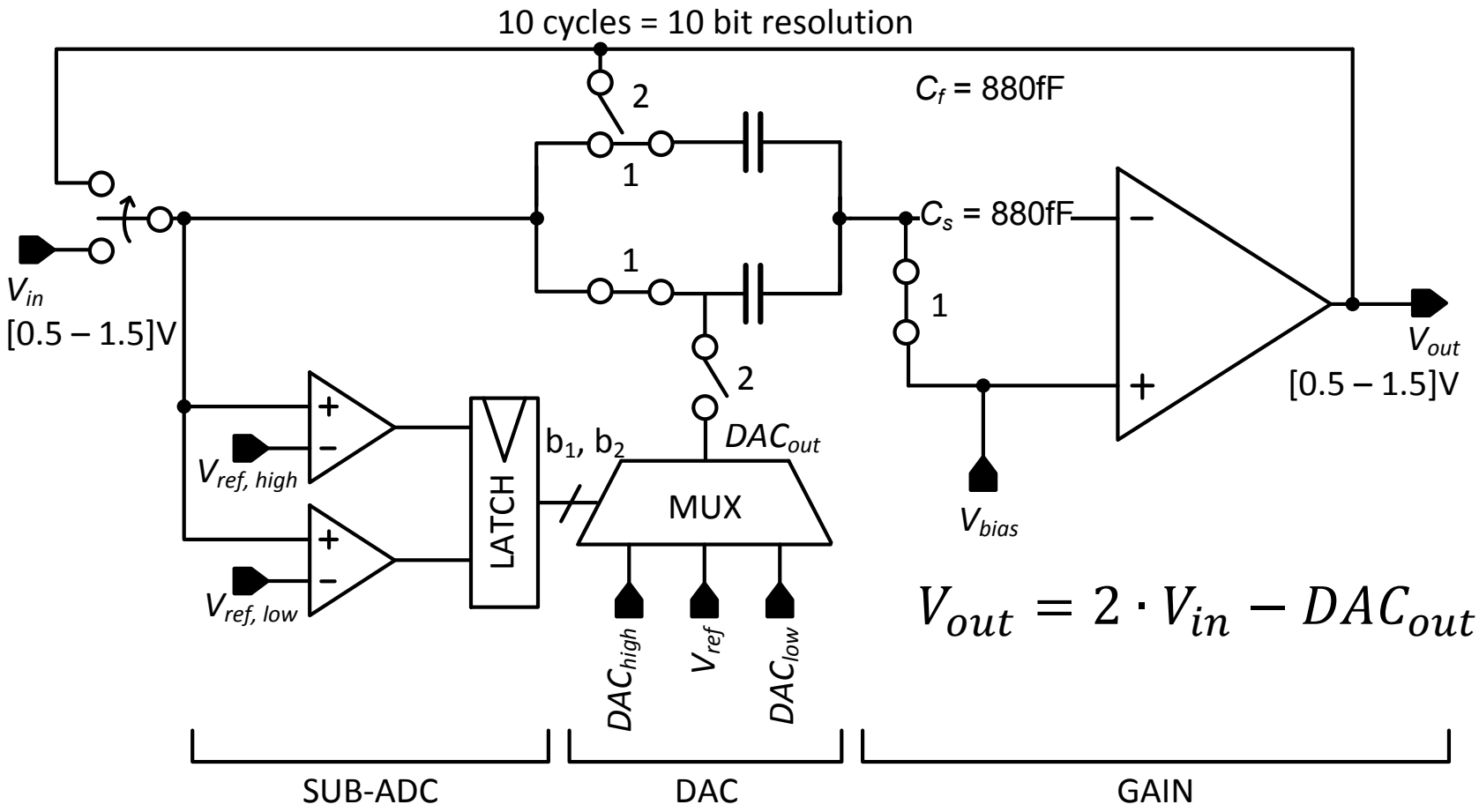
Conversion system

Concept



Conversion system

Pipelined ADC particular – Algorithmic + Digital Correction

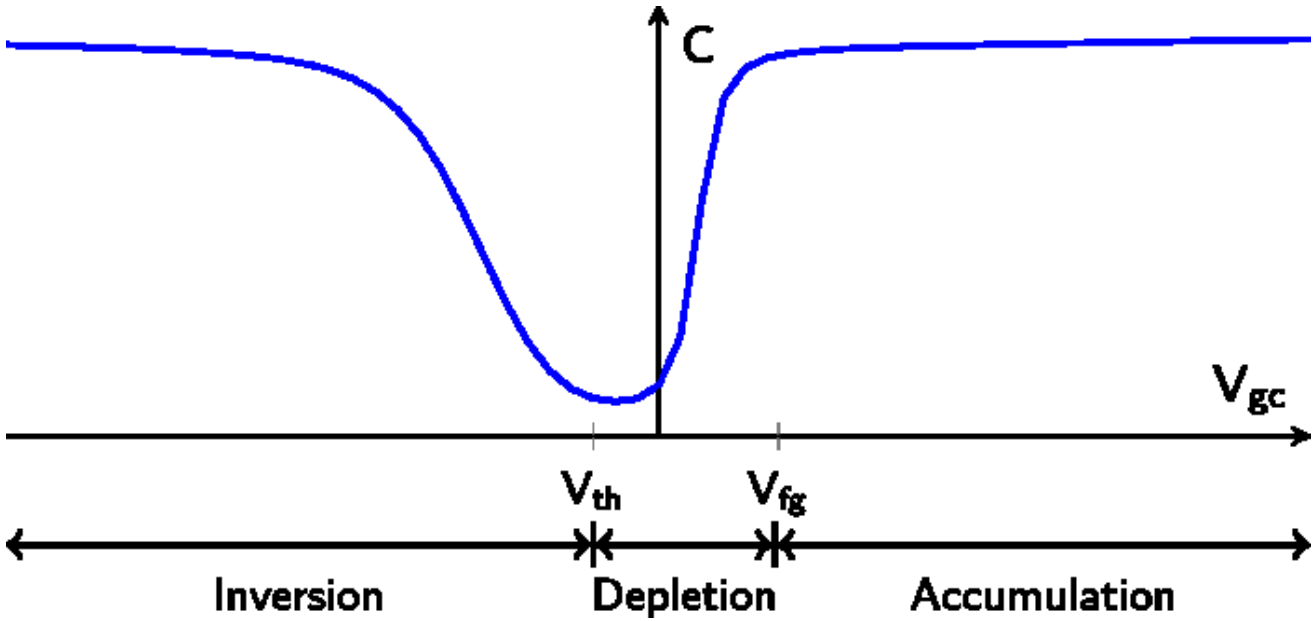


$$V_{out} = 2 \cdot V_{in} - DAC_{out}$$

Conversion system

Technological limitation

- Mismatch model not available for switched-capacitors implementation
- Linear capacitors not available



pMOS cap characteristic

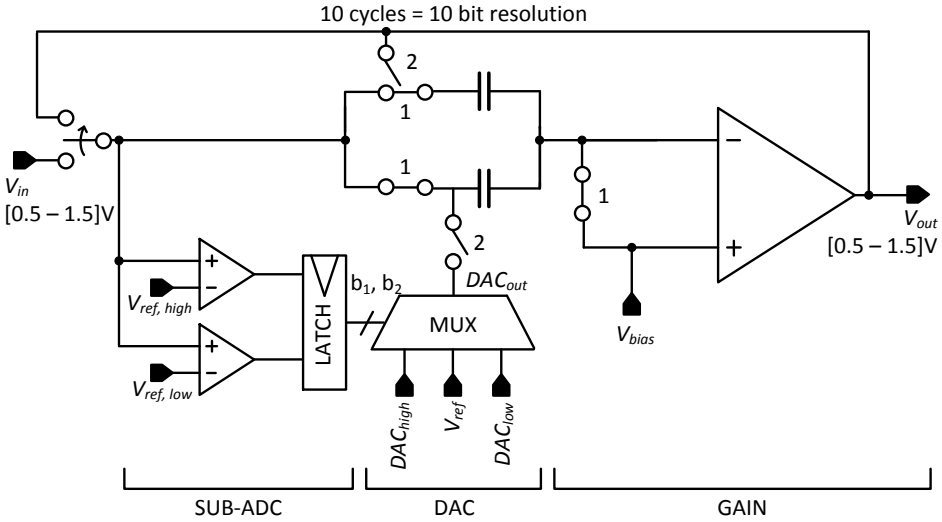
Conversion system

Design steps

- Mathematical model development with Matlab
- Transistor level design
    1) Schematic
    2) Layout
    3) Post-layout simulations
- Test chip: lab validation

Mathematical model

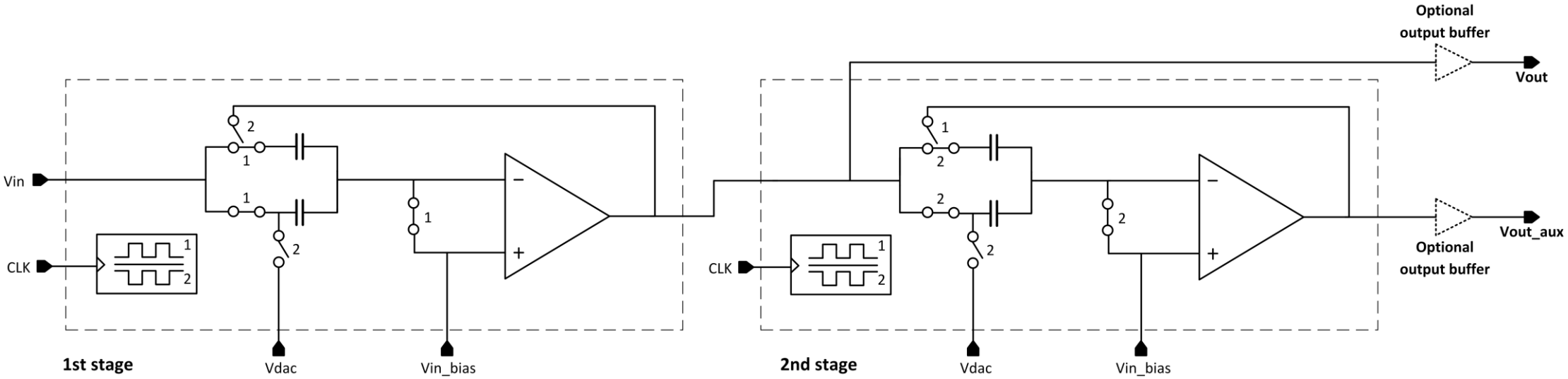
Non-idealities



- Ideally: $V_{out} = 2 \cdot V_{in} - DAC_{out}$
- In reality:
  1) Non-linear capacitors
  2) Non-ideal amplifier
  3) Mismatch
  4) References inaccuracy
- The Matlab model allows defining the required tolerance for each component
  1) Minimum amplifier gain, maximum acceptable mismatch, etc.

Transistor level implementation

Schematic implemented at transistor level



- Two stages implemented at transistor level to emulate 1 stage loaded with itself
- Main output: **Vout**
- Non-overlapping clock phases internally generated
- Two implementations available:
  1) With buffer → to evaluate the speed and transient response
  2) Without buffer → to evaluate the output DC level accuracy

Transistor level implementation

Design flow

- The circuit have been implemented in Cadence at transistor level in two versions
- The layout was drawn
- Post-layout simulations were performed in order to validate che design

Transistor level implementation

Post-Layout-Simulations results

W/O buffer		
Parameter	*Spec.*	*Result*
Vout offset	10mV	7mV @ 1 σ
Error average	< 1 LSB	< 1 LSB
Current consumption	70 µA	27 µA
W/ buffer		
Settling time (worst case)	300ns	270ns

Future outlook

- PCB design for the incoming chip
- Performs lab measurements for validation
- Explore further possible solutions for A-to-D conversion (SAR converter)
- Explore usage of this concept for wire temperature estimation